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Learning digital frequency dividers through practical laboratory activities

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Abstract

This paper present a group of useful practical activities in electronics vocational education for teaching digital frequency dividers by completing three successive stages: simulate electronic circuits with dedicated software; implement and test circuits on breadboard using general purpose logic integrated circuits; implement logic circuits using reconfigurable circuits. At the end, students will be able to implement other projects with the same level of complexity; they will have a better understanding of sequential logic circuits and good skills in working with reconfigurable circuits and handling laboratory equipment, which are essential requirements for a well-trained technician in electronic field.

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Keywords: vocational education; sequencial logic circuits; frequency dividers; practical activities; ProjectX

1. Introduction

Since the Copenhagen Declaration of 29-30 November 2002, which laid the foundations of strategic cooperation in Vocational Education and Training (VET) at the European level, many national authorities have implemented a number of European initiatives which support and improve the quality of the vocational education: European Qualifications Framework (EQF); European Credit system for Vocational Education and Training (ECVET); European Qualifications Framework (EQF); Europeas framework.

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The importance of VET is highlighted in research papers elaborated by European Centre for the Development of Vocational Training. For example, in a report in 2011 shows that "VET will continue to play an important role in the shift towards more knowledge-intensive societies" and "nearly half of the jobs in 2020 will require a medium-level qualification, which will often be achieved by some form of VET" (CEDEFOP, 2011).

However, in present, VET faces a series of problems: the large number of young people with low qualifications or no qualifications at all; technological change will increase the demand for people with medium or high qualifications; the mobility of learners in VET remains low; curriculum does not keep pace with rapid technological change; reduced investment in VET due to economic crisis.

To increase the flexibility, the quality and efficiency and attractiveness of VET, the Bruges Communiqué establish eleven strategic objectives for the period 2011-2020 and a set of short-term deliverables for 2011-2014. Among them, from this paper point of view, most important are those: "encourage practical activities and the provision of high-quality information and guidance"; "give learners in I-VET access to appropriate up-to-date to technical equipment, teaching materials and infrastructures"; "the mobility of workers and learners"; "promote active learning" and "ensure access on an equal basis" (Bruges Communiqué, 2011).

In this context, with the participation of seven country, the project "*one2one - One Teacher and One Students* working with ProjectX ", developed under European Longlife Learning Programme, aims to develop practical activities that can be done in any VET school, using a tool that was called *ProjectX*. In the meaning of *one2one* project, a *ProjectX* is "a methodological guide for the student to carry out a concrete activity, one to one with a teacher, in which theory and practice are both perfectly integrated and is related to the real workplace. Each ProjectX will be developed on the basis of Learning Outcomes, which means we will also create a tool based in the ECVET credit system that will allow mobility of students" (ProjectX, 2014).

Promoting school of each *ProjectX* should define very clearly the following aspects: ECVET level of the project; Learning Outcomes that will be achieved; time budget of the project; objectives of the theoretical part and practical part; all the tasks to be performed by students; student guide; teacher guide; all bibliographical materials needed to fulfill the projects. At the end, each *ProjectX* will be evaluated and implemented by other partners, in order to improve the quality and transferability of the project.

2. Project description

In the frame of *one2one* we design and promote one *ProjectX* related to the study and implementation of frequency dividers taking into account that these circuits are basic blocks in almost any modern digital equipment, from traffic lights to computers. A good understanding of these circuits is essential for well-trained technician in electronic field.

Also is very important for the future technician in this field to be able to use alternative ways to implement any logic circuit such as: classic way - using general purpose logic integrated circuits (IC); or in the modern way - based on reconfigurable logic IC such as Field Programmable Gate Array (FPGA).

Regarding new trend in digital electronics, in our opinion, in the near future, it will be difficult to find any high performance digital systems without FPGA inside of it. So, we think it is very important to teach students how to use these circuits in order to cope with technological changes in this field. We believe that teaching how to use FPGA should not remain only at academic level; we think it is time to introduce them in VET curricula for medium level of qualifications.

This section describes the main theoretical and practical aspects related to the study and implementation of frequency dividers in the vocational education with medium or high level of qualification.

2.1. Previous knowledge of the theoretical part

In the theoretical part, which represent about one third of the time budget of the project, we gradually introduce well selected tutorials and exercises to improve students' previous theoretical knowledge about flip-flops and counters. For both types of logic circuits we are focused more on how to use and less on how is made inside.

Because counter is the key component in any divider, increased attention must be given for a very good understanding of all aspects regarding counters operation; it is vital for students to understand the special functions such as parallel load, count enable, reset and external signaling of terminal counting situations (Floyd, 2006), (WiscOnline, 2014).

Also we find that is very important to make another step towards practical applications: to teach students how to use datasheet in order to convert a logical diagram into a wiring diagram which can be implemented with general purpose logic IC.

2.2. Frequency dividers design techniques

After a deep understanding of how counter works, we have the foundation to start teaching frequency dividers. From many frequency dividers know in present, based on our experience, we selected only four representative types which will be introduced gradually by means of well selected examples.

2.2.1. Frequency dividers

The first design method is based on using a counter reset function as can be seen in Figure 1 for a particular case in which division factor is equal to 12. This method requires three steps and is easily understood by students. As presented in Figure 1.a, the first step start by choosing a generic 4-bit binary counter, by writing all states of the counter in their normal sequence and then by splitting them in two parts: allowed states (the first 12 states - state 0 to state 11) and interdicted states (the rest of the states, state 12 to state 15). In the second step, an external logic is designed to clear the counter when we detect the first interdicted state of the counter (Figure 1.b). In final step we convert logical diagram into wiring diagram with general purpose IC (Figure 1.c). For these types of dividers we can control the division factor but we don't have control over duty-cycle of the output signal.

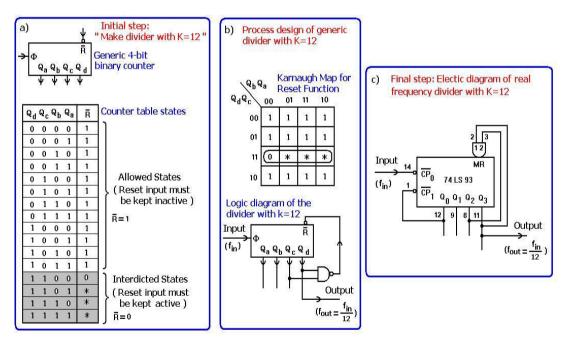


Fig. 1. Design divider using asynchronous counter (a) making truth table; (b) design logic diagram; (b) design wiring diagram.

2.2.2. Programmable frequency dividers - type 1

The second group of methods no longer uses the reset function of the counters; these are based on synchronous counters with parallel load capability and terminal counting outputs, such as 74LS193 or 74LS192. Briefly speaking, the counter is loaded with divider factor and then is putted to count down until reach zero state, moment in which Terminal Count Down (TCD) output become active. Through an external wire connection, TCD output activation is converted into a new command of parallel load of the counter. After this command, the counter is loaded with divider factor and TCD output is deactivated. From this point the counter can count down from the factor just loaded to zero and then the operation is repeated.

Note that the division factor of these frequency dividers is decided by the numerical information applied on parallel inputs of the counter when we have an active parallel load command. So, if we change the data applied on parallel inputs we change the division factor of the divider, without modifying the wiring diagram of the divider. From this reason, these dividers are called programmable frequency dividers.

Programmable frequency dividers are more difficult to understand and should be introduced gradually from simple to complex and should be explained in great detail because there are many phenomena which have a very rapid succession. In the tests performed with our students we conclude that it is better to be delivered on 3 levels of complexity.

For the first type of programmable frequency divider we suggest examples similar to those shown in Figure 2. Here we have a two-decade BCD counter which operates as a programmable divider with factor equal to 74. It is preferable to start teaching with scheme in Figure 2.a, although it has some problems due to asynchronous loading of the counter, and then shows how these problems are eliminated by using a latch implemented with P2 and P3 gates, as shown in Figure 2.b. Note that after latch introducing the division factor increases by one unit therefore in order to maintain the same division factor, in this case 74, it is necessary to apply 73 on parallel data inputs of the counters.

These dividers have two major drawbacks: generates output signals with very short logical zero and not allow the duty cycle control.

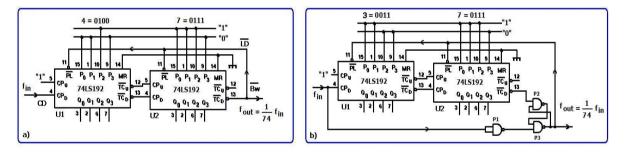


Fig. 2. First type of programmable frequency dividers (a) without latch; (b) with latch.

2.2.3. Programmable frequency dividers - type 2

At the next level are discussed programmable dividers that allow a reduced control of the duty-cycle of the output signal. For these types of dividers, in addition to the previous diagrams, hire we find one flip-flop which is switched each time when counters goes through zero state. The outputs of flip-flop are used to change the binary data applied on parallel inputs of the counters, which means it change the division factor. More specifically, if flip-flop is high counters are loaded with one constant and if is low counters are loaded with another constant.

For example presented in Figure 3, one constant is $N=0101100_{BCD}$ for high state of the flip-flop and other constant is $M=0001100_{BCD}$ for low state of the flip-flop. In these conditions, the output signal will be logic high for 58+1 periods of the input signal and will be logic low for next 14+1 periods. We can conclude that the period of the output signal is equal to 74 periods of the input signal, which means that the frequency division factor is equal to 74.

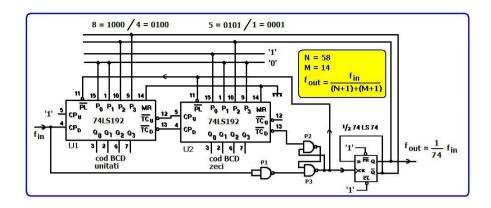


Fig. 3. Second type of programmable frequency divider using flip-flop to modify numeric information applied on parallel inputs.

The main disadvantage of the divider shown in Figure 3 is the fact that the two constants M and N cannot be completely different, which means that we cannot achieve any duty-cycle we want.

2.2.4. Programmable frequency dividers - type 3

The third type of programmable divider is the most flexible in the sense that we can control both the division factor and the duty-cycle of the output signal. The block diagram in Figure 4 reveals that the flip-flop output is used to control the select lines of the 2 to 1 multiplexers. In this way we are able to operate with any value for the constants M and N, since they are outside and are not influenced by the flip-flop state.

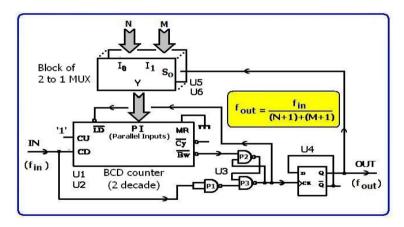


Fig. 4. Bloc diagram of the third programmable frequency divider - general case.

Usually, this kind of divider is the most difficult to understand and can be done only by advanced students, for high grades.

2.3. Practical activities – Implementation of the frequency dividers with general purpose logic IC

In the practical part of the *ProjectX*, representing the remaining two thirds of the time budget, we identified three types of practical activities to be completed by each student: simulate an electronic circuit with dedicated software

programs; implement and test simple sequential circuits, on breadboard, with standard logic IC; implement simple electronic circuits using modern digital circuits such as FPGA.

In order to be able to implement and test the divider in real world, each student must convert the logic diagram into wiring diagram through a series of intermediate activities: choose the right commercial logic ICs; make right allocation of internal resources of the IC to cover all components of the logic diagram; decide what to do with unused resources or unused IC pins; make connection between pins; specify pins for power supply; specify the number of pin and the number of IC for each logic symbol.

After completing the wiring diagram, before moving on to the practical circuit verification, is recommended to use a dedicated simulation program such as SPICE for circuit verification. Performing simulations in electronics field is a common practice because it allows comfortable viewing of electrical signals from several points of the scheme. In our experiments we successfully use Tina-Pro software because is easy to use, has a lot of virtual instruments, has interactive simulation and student edition is free (DesignSoft, 2014). One typical use of this software is presented in Figure 5.a, for a frequency divider implemented with asynchronous counter.

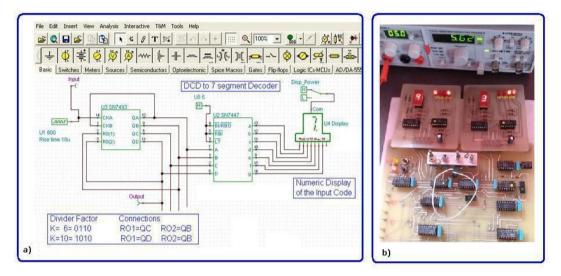


Fig. 5. Practical activities for divider implementation: a) simulation; b) implementation on PCB with general purpose logic IC

The last step in practical activities is dedicated to practical realization of the dividers which was previously studied and simulated. At the beginning is useful to work with breadboards but the ultimate goal of each student is to make the printed circuit board (PCB), similar with board presented in Figure 5.b.

2.4. Practical activities – Implementation of the frequency dividers with FPGA

Nowadays there is a tendency of increased use of FPGA in the implementation of digital systems due to the advantages of these circuits (National Instruments, 2012): reconfigurability, small size and great performances at low power and low cost, rapid prototyping, mature software development environments.

From student point of view, FPGA can be seen as a chip with a huge numbers of logic gates, flip-flop, little blocks of memory and other logic circuits which are not connected in factory. To implement a logic circuit in FPGA students must perform the following steps: description of the logic function that they want to implement; compile the logic function to obtain a binary file (bitstream) that can be downloaded into the FPGA; circuit configuration using connection cable between PC and FPGA board; testing the application; in case of mistake students must fix the logic function, re-compile and re-download it.

It is important to note that current development environments allow a large number of possibilities for describing logic function of the circuit (Xilinx, 2014). In our experiments, for low level of qualification, we used schematics and, for midlevel of qualification, we successful use VHDL hardware description language.

This group of practical applications is the most attractive for students because they design a hardware product in a manner that is very similar to make a software program. They "can configure these chips to implement custom hardware functionality without ever having to pick up a breadboard or soldering iron" (National Instruments, 2012).

3. Learning outcomes of the project

To be easily integrated in VET system of different European countries, each group of practical activities developed under the name *ProjectX* must present, besides detailed description of theoretical and practical activities, a list of skills and abilities acquired after project completion. If these learning outcomes are attractive and are in compliance with the requirements for a particular qualification, we have a chance to increase the degree of mobility in VET systems.

In Table 1 are listed the main skills related to the design and simulation of logic circuits, in Table 2 are shown the main skills related to circuit implementation using general purpose logic IC and their testing. Finally, in Table 3 are described skills acquired in the design and implementation of logic circuits using FPGA.

Table 1. Skills related to circuit design and circuit simulation.

Circuit design		Circuit simulation	
-	understand initial technical specifications;	-	draw the electrical diagram of the circuit
-	choose the right method to design the logic diagram of the divider;	-	choose the right type of analysis;
-	design the logic diagram;	-	display electrical signals in different points of electrical diagram; use virtual instruments
-	convert the logic diagram into wiring schematic;		
-	choose the right logic ICs,	-	
-	make right allocation of internal resources of the IC to cover all components of the logic diagram;		
-	make right connections for unused IC pins;		

Table 2. Skills related to implementation and test the electronic circuit with general purpose logic IC.

Skills related to circuit implementation		Skills related to circuit test	
-	make a bill of materials;	-	check the correct realization of the electrical diagram;
-	identify the ICs needed to construct the schematic;	-	make right connection to signal generator and power supply;
-	make connection between pins;	-	use oscilloscope to display the input/output electrical signals.

Table 3. Skills related to implementation of logic circuit with FPGA .

Circuit design with FPGA		Testing circuits implemented in FPGA	
-	make new project, add new sources into project, draw the schematic of the divider; make constrains file (specify the input/output FPGA pins);	 download the configuration file into FPGA; make connection to the signal generator and power supply; make tests to verify the functionality of the circuit. 	
-	generate configuration file;	- use oscilloscope to display the input/output electrical signals	

At the end of this *ProjectX*, we can conclude that all students will be able to simulate, design and implement other projects like: electronic clocks, programmable timers, events counting systems and so on. Also, they have already learned two alternative ways to implement any logic circuit: the classical way (based on general purpose logic IC) and the newest and modern way (based on reconfigurable logic IC, such as CPLD or FPGA). They will have a better understanding of sequential logic circuits, good skills in operating with laboratory equipment and good

skills in operating with reconfigurable circuits which are essential requirements for a well-trained technician in electronic field.

4. Conclusion

In this paper were presented a series of theoretical and practical activities useful for VET, in order to improve general knowledge about sequential logic circuits and also provides detailed steps in order to design and implement four different types of frequency dividers.

All these activities are designed to bring the following benefits to students who complete this project:

- Have a better understanding of sequential logic circuits such as flip-flops and counters;
- Design three different type of frequency dividers based on asynchronous/synchronous counters;
- Convert a generic logical diagram into a wiring diagram using general purpose logic IC;
- Use computer programs to simulate any small/medium digital circuit designed by them or designed by other;
- Use breadboard and general purpose logic IC to implement and test any small/medium logic circuit;
- Use state of the art logic IC such as FPGA to implement small/medium logic circuit;
- Improve personal skills in handling laboratory equipment and computer use.

At the end of these activities, students will be able to design and implement, on their own, other projects with similar complexity such as: electronic clocks, programmable timers or events counting systems. Also, they have already learned two complementary methods to implement a logic circuit using either general purpose logic IC or reconfigurable logic IC such as FPGA.

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